

| | L # | Hits | Type | Search Text | DBs | Time Stamp |
|---|-----|------|------|------------------------------------|-----------------------------------|------------------|
| 1 | L1 | 0 | BRS | North adj brigde | USPAT; EPO; JPO; IBM TDB | 2001/07/15 15:41 |
| 2 | L2 | 147 | BRS | North adj bridge | USPAT; EPO; JPO; IBM TDB | 2001/07/15 15:42 |
| 3 | L3 | 7 | BRS | (North adj bridge) same timing | USPAT; EPO; JPO; IBM TDB | 2001/07/15 15:46 |
| 4 | L4 | 2 | BRS | (North adj bridge) same refresh\$3 | USPAT; EPO; JPO; IBM TDB | 2001/07/15 15:46 |

| | Document ID | Issue Date | Pages | Title | Current OR | Current XRef |
|---|--------------|------------|-------|---|------------|-----------------------------|
| 1 | US 5857085 A | 19990105 | 15 | Interface device for XT/AT system devices on high speed local bus | 710/129 | 710/126 710/128 |
| 2 | US 5935226 A | 19990810 | 12 | Method and apparatus for issuing transaction requests to a target device in accordance with the state of connection between the portable computer and the target device | 710/101 | 710/129 |
| 3 | US 6085330 A | 20000704 | 9 | Control circuit for switching a processor between multiple low power states to allow cache snoops | 713/322 | 711/146 711/3 713/300 |
| 4 | US 6094700 A | 20000725 | 21 | Serial bus system for sending multiple frames of unique data | 710/129 | 710/30 |
| 5 | US 6098174 A | 20000801 | 9 | Power control circuitry for use in a computer system and systems using the same | 713/300 | 365/229 713/310 |
| 6 | US 6134167 A | 20001017 | 25 | Reducing power consumption in computer memory | 365/222 | 365/229 |
| 7 | US 6134625 A | 20001017 | 14 | Method and apparatus for providing arbitration between multiple data streams | 710/241 | 710/129 |

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|---|--------------|------------|-------|---|------------|--------------------|
| 1 | US 6098174 A | 20000801 | 9 | Power control circuitry for use in a computer system and systems using the same | 713/300 | 365/229 713/310 |
| 2 | US 6167486 A | 20001226 | 17 | Parallel access virtual channel memory system with cacheable channels | 711/120 | 711/123 711/150 |